Z86017/Z86M17

PCMCIA Interface

Preliminary Customer Procurement Specification

PS011101-0601

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Document Disclaimer

Z86017/Z86M17
PCMCIA INTERFACE

FEATURES

Part	RAM* (Bytes)	Speed (MHz)
Z86017	256	20
Z86M17	256	20

*Attribute

Translation Capabilities

- PCMCIA to IDE Translation
- IDE to IDE Mapping, Pass Through Mode
- Direct Memory Access (DMA) Support

Supports Multiple Applications

- 256 Bytes of Attribute Memory
- Five Configuration Registers
- Three Additional Registers to Support EEPROM Programming
- Three Programmable Memory or I/O Map Ranges
- Conforms to PCMCIA Standards
- EXCA Register Compatible

GENERAL DESCRIPTION

The Z86017 is a general-purpose PCMCIA adaptor chip used on the card side of the interface. The Z86017 easily configures to all types of memory and I/O mapped peripheral hardware. Mapping is performed from the I/O and Memory mapped PCMCIA to local peripheral ICs that support Ethernet controllers, UARTs, modems, printer ports, solid state memory, rotating disk memory, and other peripheral devices.

The Z86017 can be used in a stand-alone configuration without the use of a local processor by providing all of the attribute memory, CCRs, range, interrupt types through a serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The Z86017 can also be configured through a local processor for use on intelligent controller systems.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

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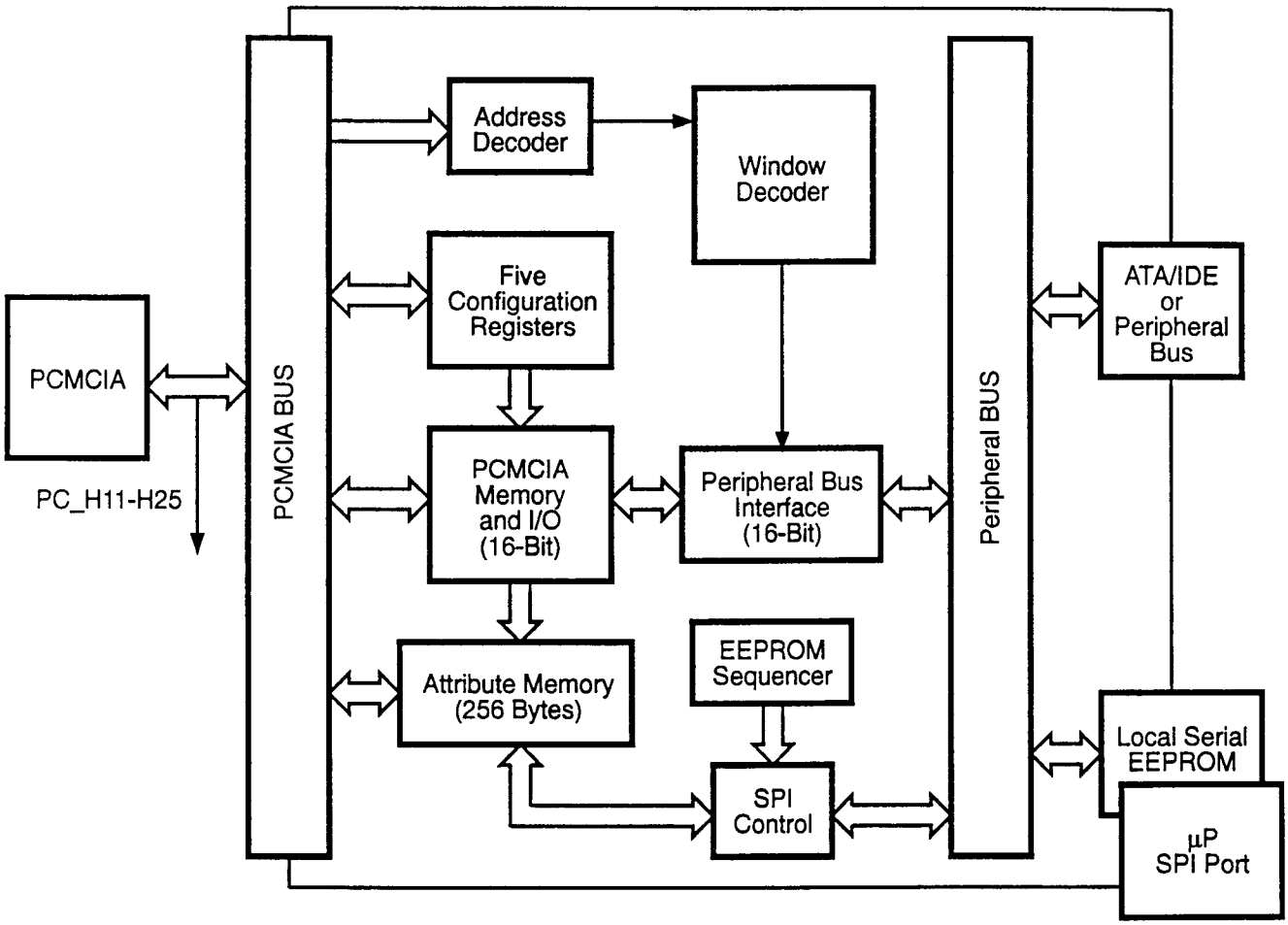
GENERAL DESCRIPTION (Continued)

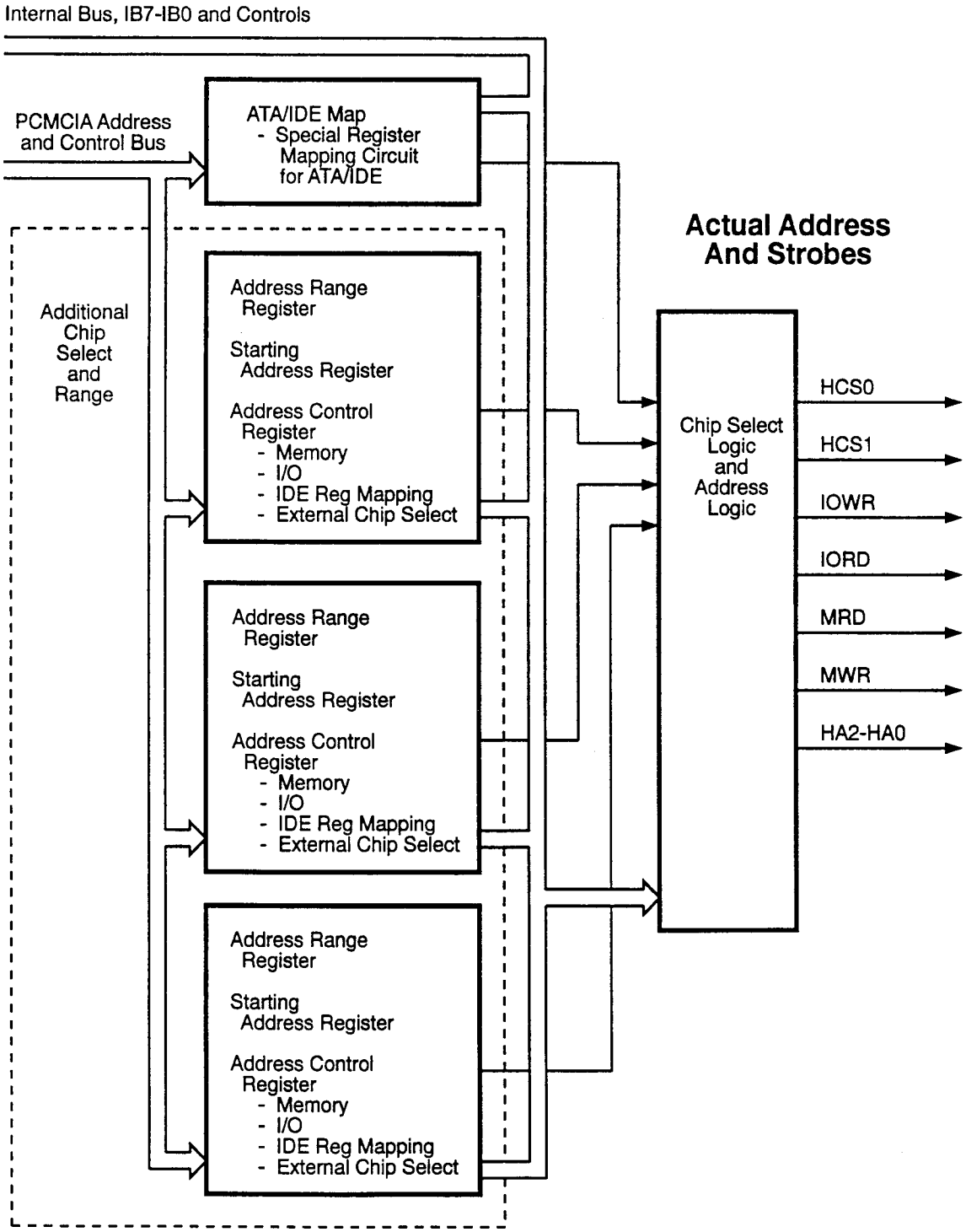
The local processor connects to the Z86017 through the serial interface or can be programmed through an external EEPROM. The Z86017 provides for the PCMCIA to ATA/IDE translation, ATA/IDE to ATA/IDE mapping, or PCMCIA to three general-purpose maps.



Z86017 Functional Block Diagram

The Z86017 supports three general-purpose maps and one special map for PCMCIA to ATA/IDE Transactions .

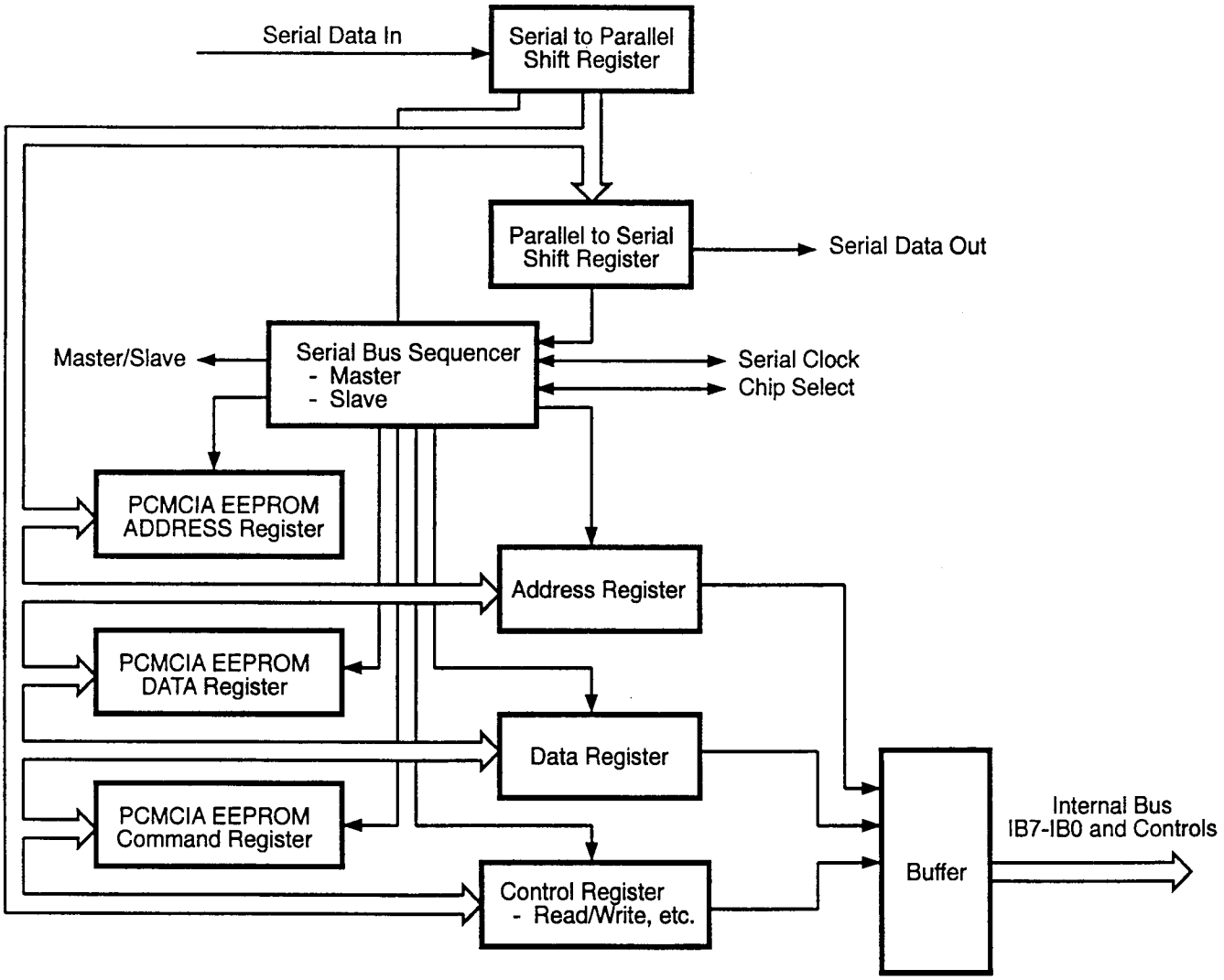
Address Mapping Circuit



Connection Block Diagram

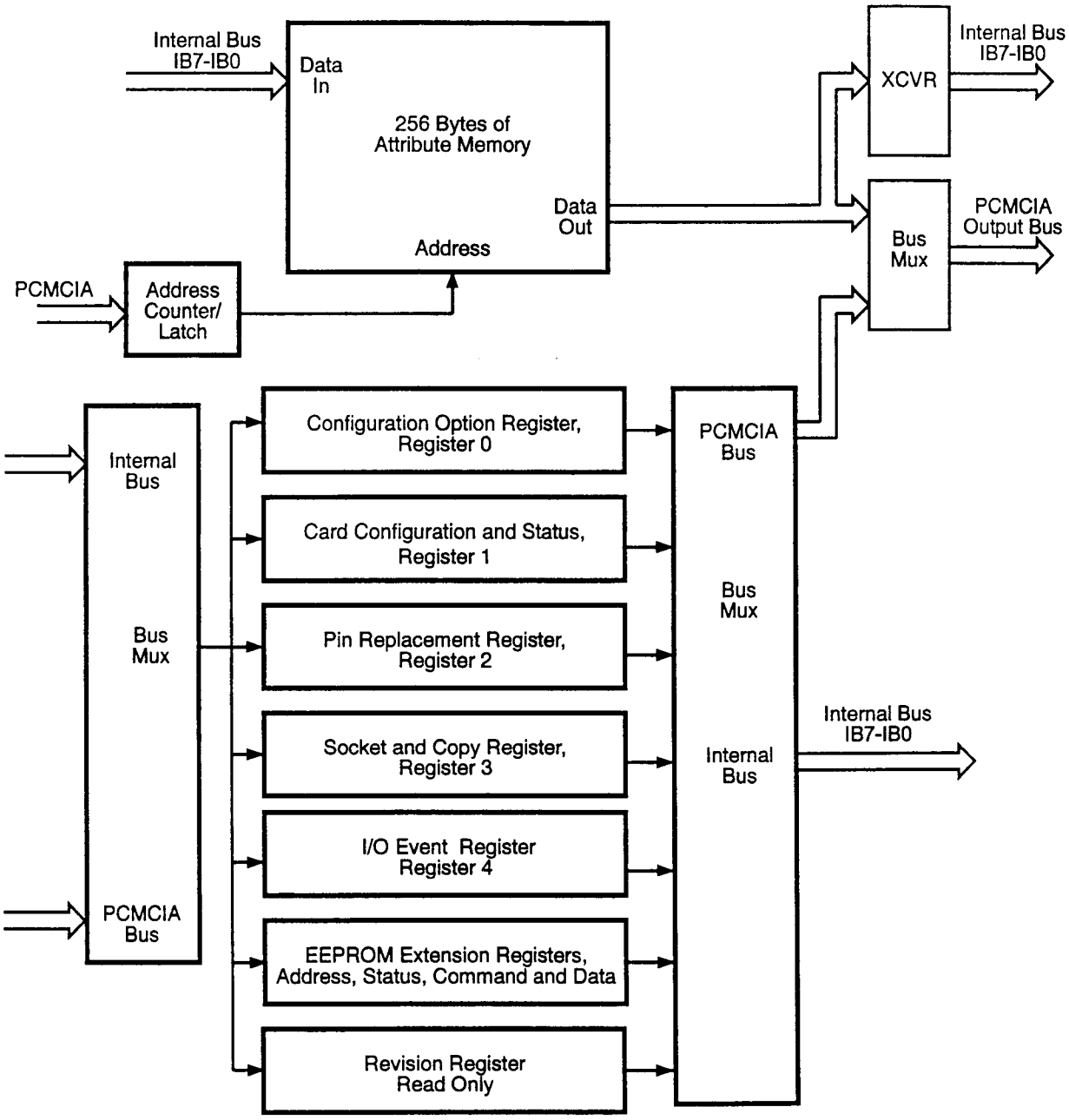
GENERAL DESCRIPTION (Continued)

The Z86017 IC can become an EEPROM interface master or a local processor slave. There are two independent sequencer circuits in the IC to provide for the master and slave operation.



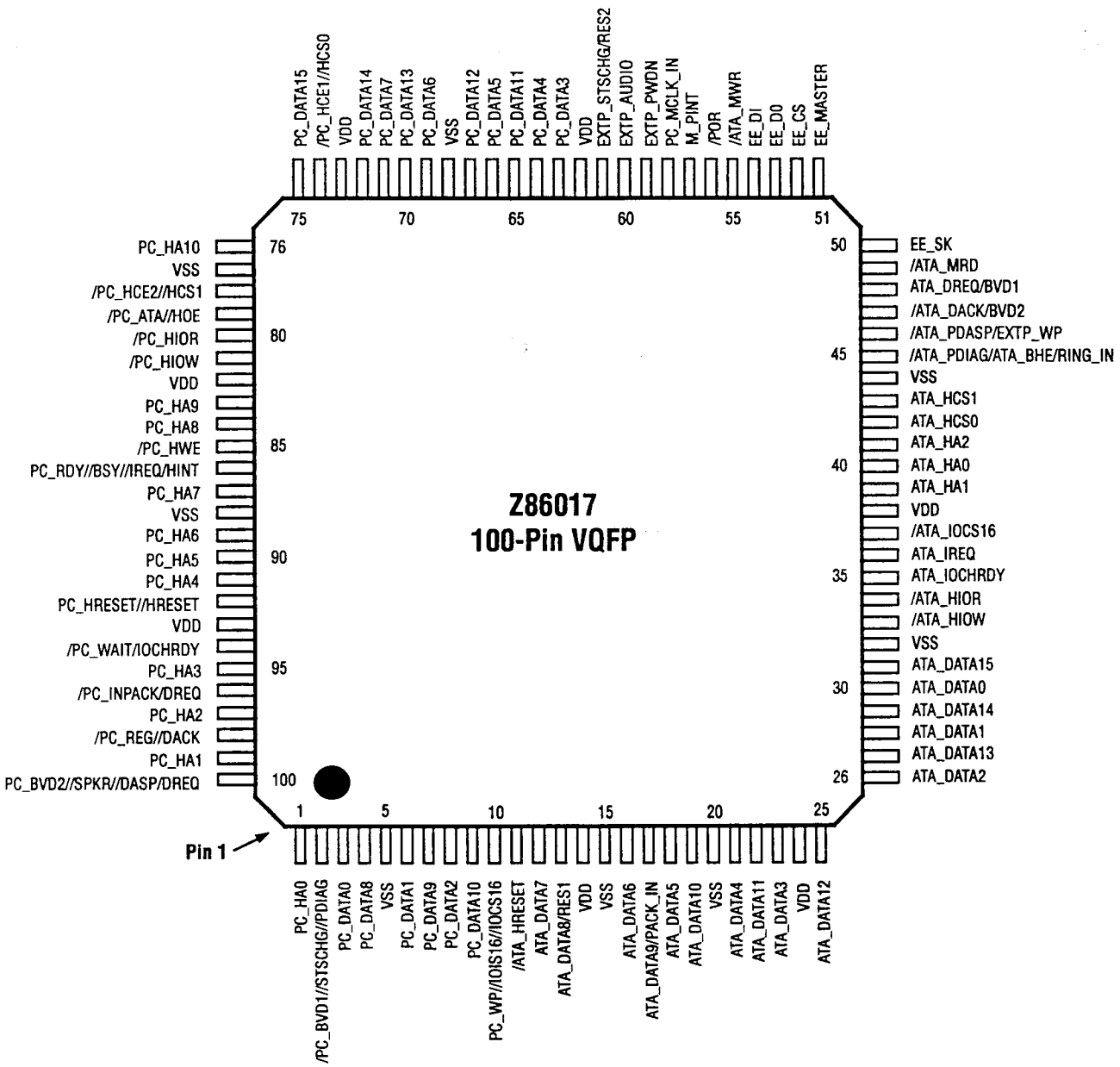
Serial Interface Diagram

The Z86017 IC provides the five standard PCMCIA registers. Four additional registers have been added to provide for remote programming of the EEPROM and Revision Control Status Information.

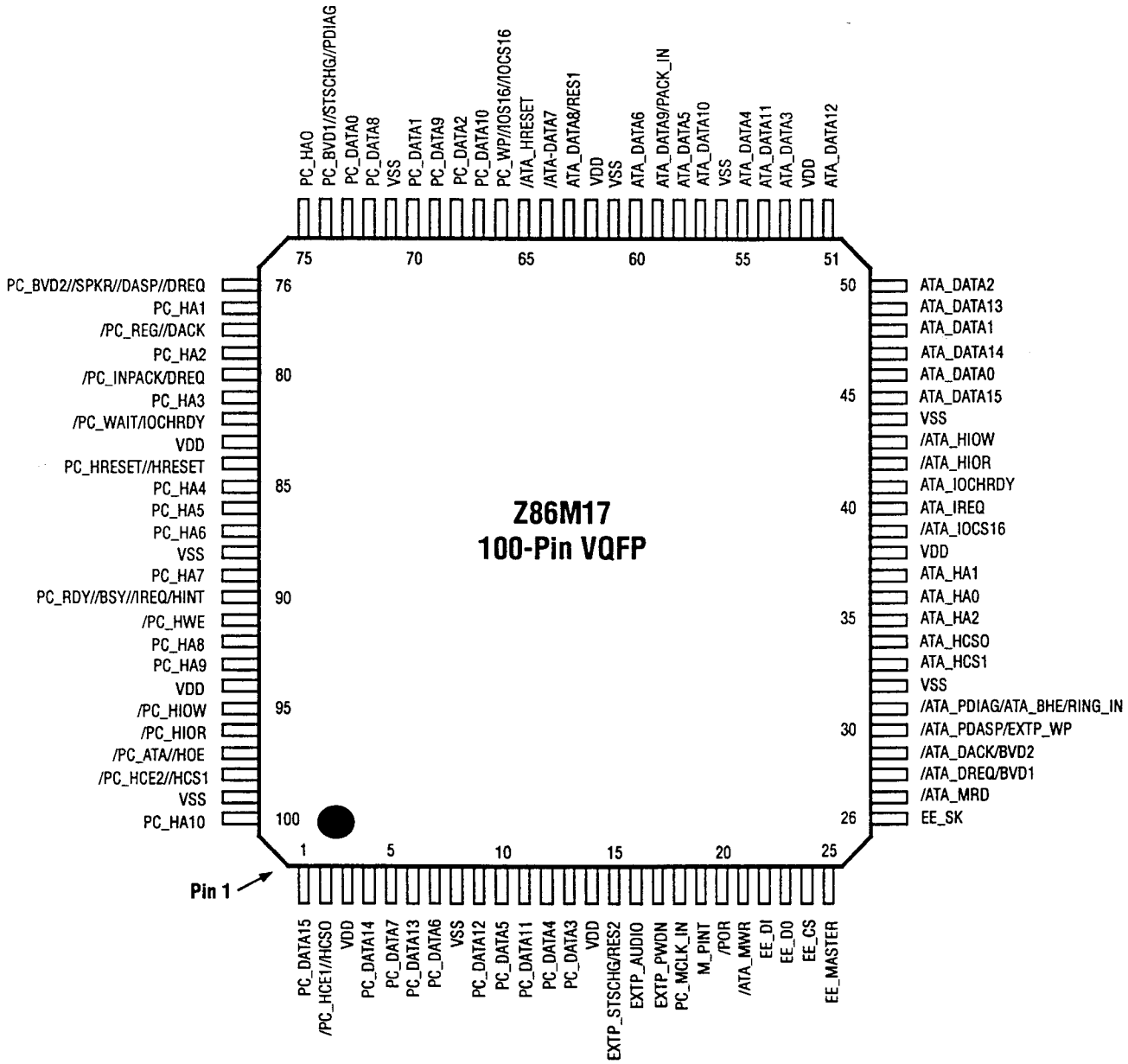


Attribute and Configuration Memory Diagram

PIN DESCRIPTION



Z8601720ASC 100-Pin VQFP Package



Z86M1720ASC 100-Pin VQFP Package

ABSOLUTE MAXIMUM RATINGS

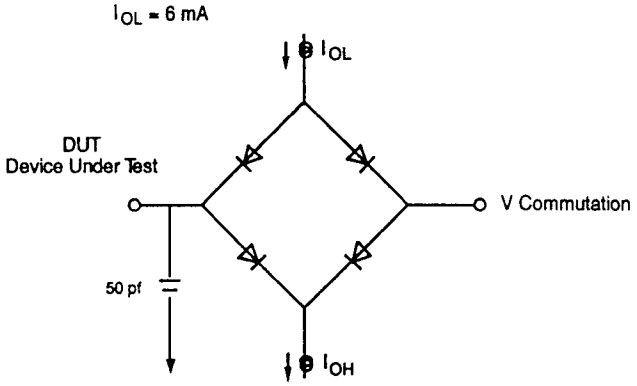
Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65	+150	C
T_A	Oper. Ambient Temp.	0°	+70°	C

* Voltages on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted (Test Load Diagram).



Test Load Diagram

DC SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min Value	Max Value
Supply Voltage	V_{DD}	V	–0.5	7.0
Input Voltage	V_I	V	–0.5	V_{DD} + 0.5
Output Voltage	V_O	V	–0.5	V_{DD} + 0.5
Storage Temperature	T_{STG}	C	–40	+125
Temperature Under Bias	T_{BIAS}	C	–25	+85

5.0V Operating Conditions

Parameter	Symbol	Unit	Min Value	Typical	Max Value
Supply Voltage	V_{DD}	V	4.5		5.5
Input High Voltage for TTL Inputs	V_{IH}	V	2.4		V_{DD}
Input Low Voltage for TTL Inputs	V_{IL}	V	–0.5		0.8
*Input Low Voltage for Schmitt-Triggered Inputs	V_{IL}	V	–0.5	0.8	
Operating Temperature	T_A	°C	0		70

* Schmitt-Triggered Inputs - PC_HRESET//HRESET, /POR, PC_MCLK_IN

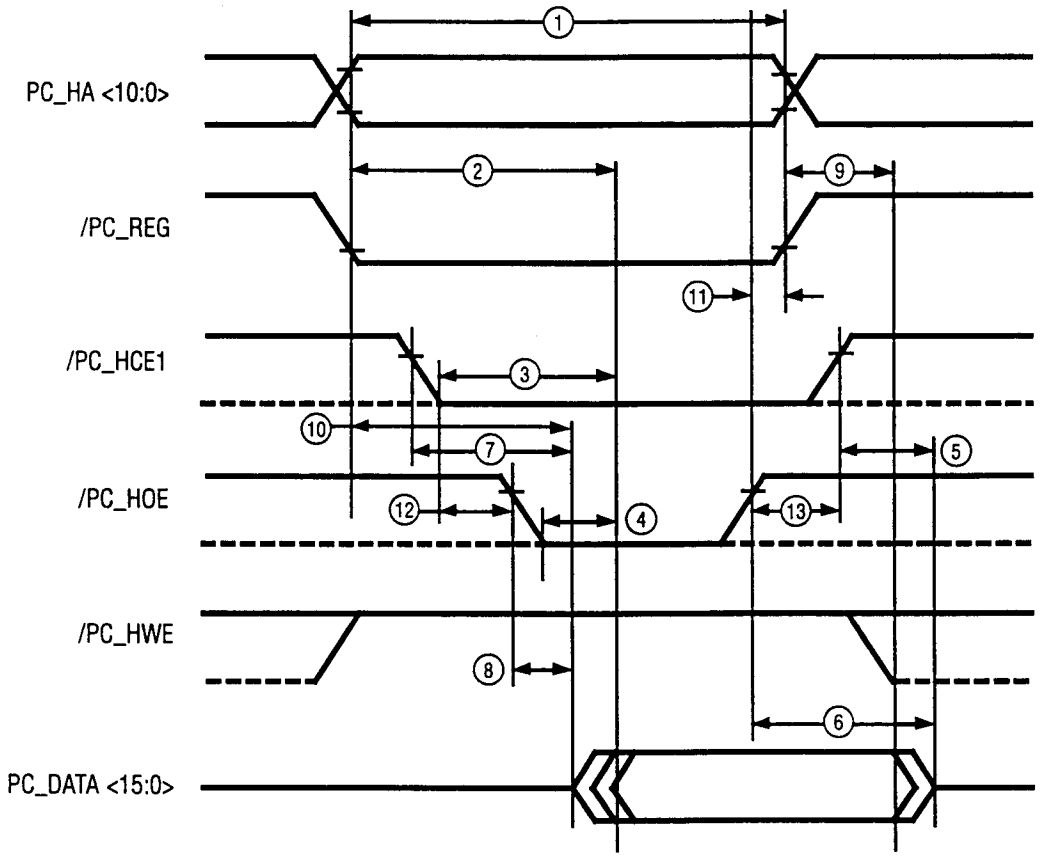
DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Unit	Min Value	Max Value
Power Supply Current (1)	I_{DDS}	mA		5 (@ 5V)
Output High Voltage	V_{OH} (I_{OH} = –6 mA)	V	2.4	V_{DD}
Output Low Voltage	V_{OL} (I_{OL} = 6 mA)	V		0.4
Input Leakage Current	I_L $V_I \le V_{DD}$	µA	–10	10
Power Dissipation	P_{MAX}	mW		25 @ 5V
	Power Down Mode (2)	mW		2.5 @ 5V
Input Capacitance	C_I	pF		8 pF

Note:
(1) Inputs driven to 0V outputs floating PC_MCLK_IN=20 MHz, EE_SK=0
(2) EN_PADs bit set and PC_MCLK_IN = 0, EE_SK = 0

INTERNAL ATTRIBUTE MEMORY TIMING
(Speed Version: 300 ns)

No	Symbol	Parameter	Min	Max	Units
1	TcR	Read Cycle Time	300		ns
2	TaA	Address Access Time		300	ns
3	TaCE	Card Enable Time		300	ns
4	TaOE	Output Enable Access Time		150	ns
5	TdisCE	Output Disable Time from CE		100	ns
6	TdisOE	Output Disable Time from OE		100	ns
7	TenCE	Output Enable Time from CE	5		ns
8	TenOE	Output Enable Time from OE	5		ns
9	TvA	Data Valid from Address Change	0		ns
10	TsuA	Address Setup Time	30		ns
11	ThA	Address Hold Time	20		ns
12	TsuCE	Card Enable Setup Time	0		ns
13	ThCE	Card Enable Hold Time	20		ns
14	TvWToe	Wait Valid from OE		35	ns
15	TwWT	Wait Pulse Width		12	µs
16	TvWT	Data Setup for Wait Released	0		ns



Note: /PC_REG is active Low for Attribute Memory reads only.

PCMCIA Read Memory Timing, No Wait States

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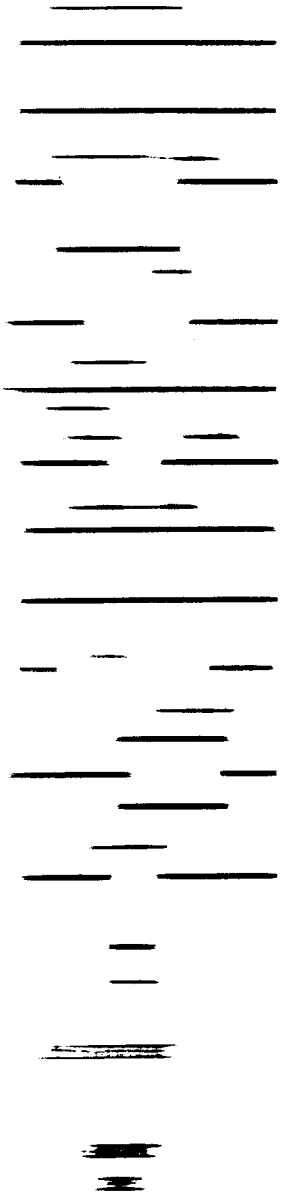

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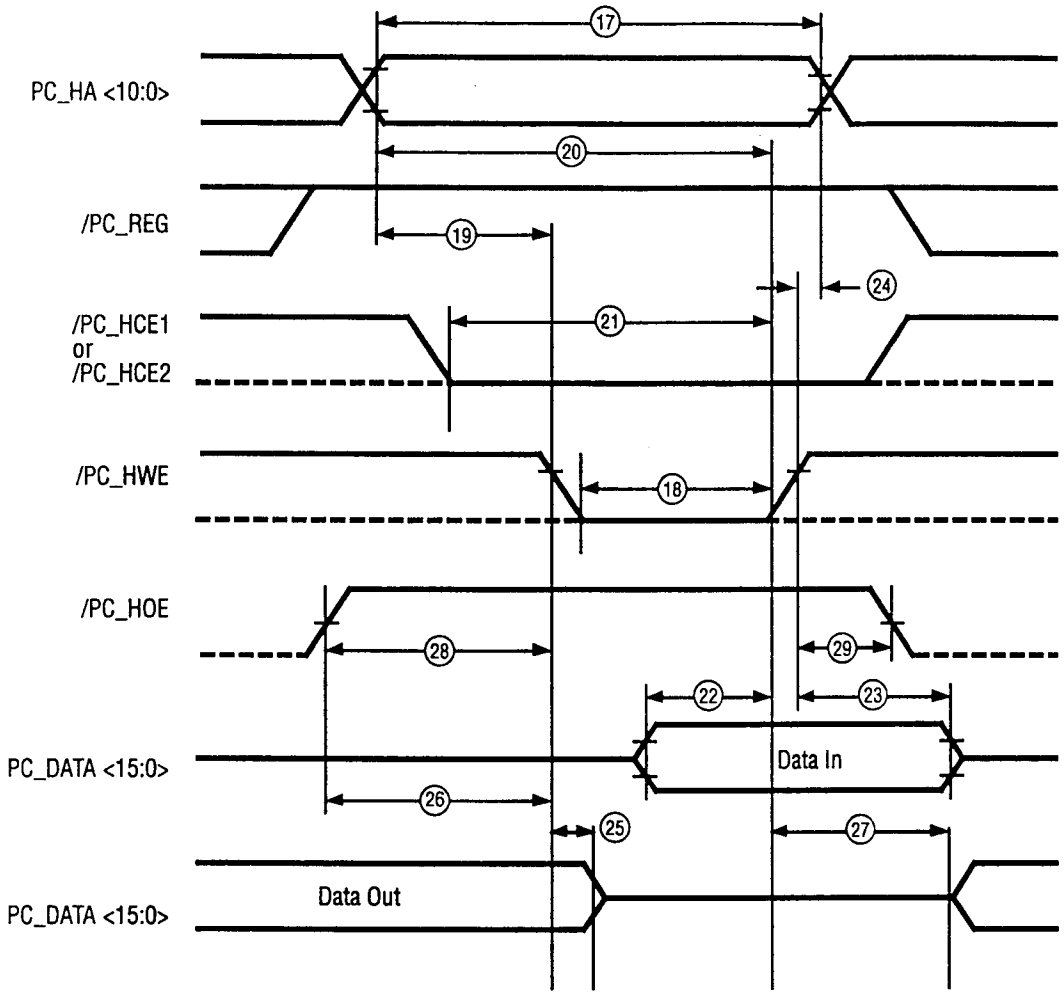
PCMCIA MEMORY WRITE TIMING

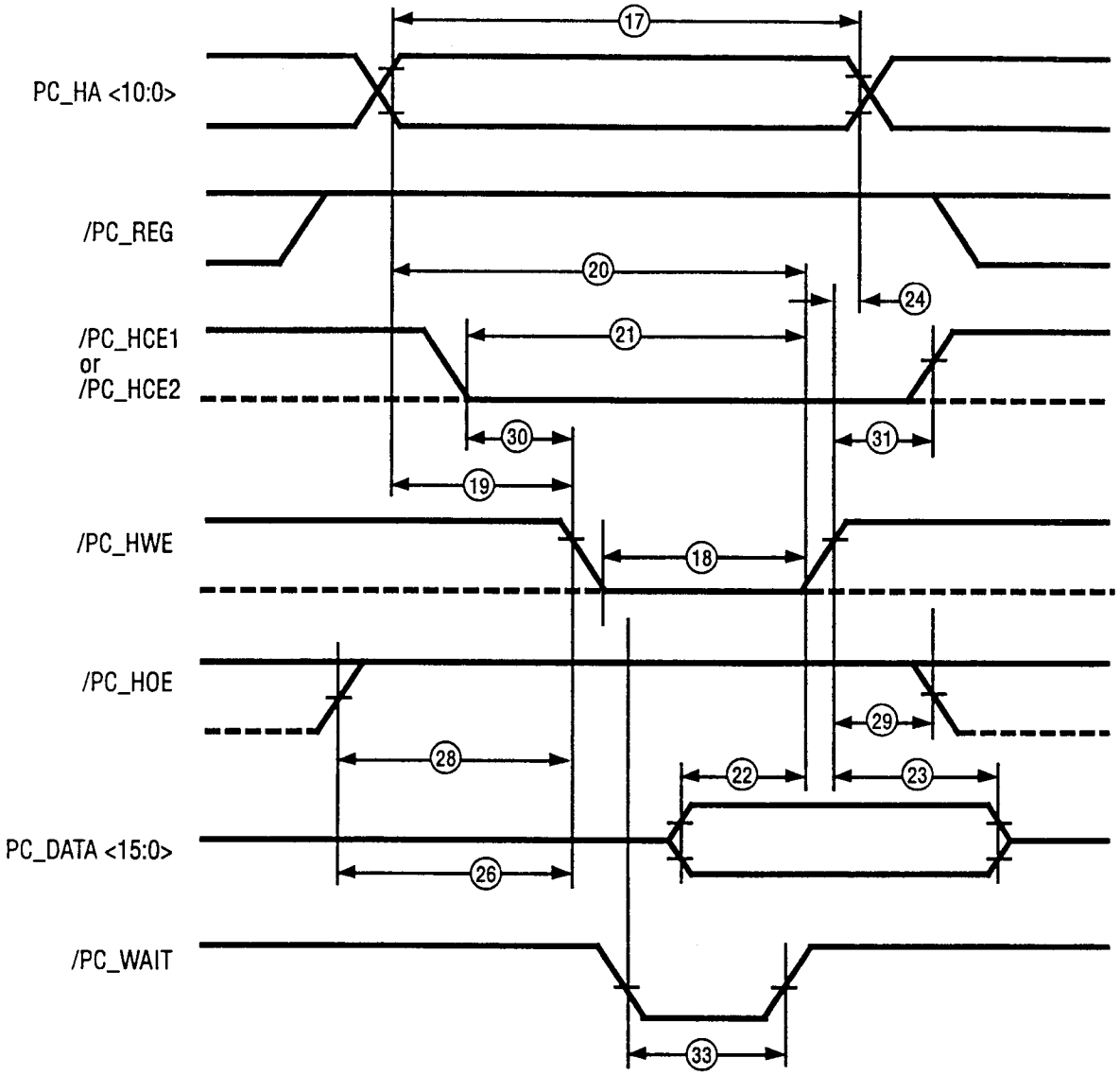
No	Symbol	Parameter	200 ns Min	200 ns Max	150 ns Min	150 ns Max	100 ns Min	100 ns Max	Units
17	TcW	Write Cycle Time	200		150		100		ns
18	TwWE	Write Pulse Width	120		80		60		ns
19	TsuA	Address Setup Time	20		20		10		ns
20	TsuAwe	Address Setup Time for WE	140		100		70		ns
21	TsuCwe	Card Enable Setup Time for WE	140		100		70		ns
22	TsuDwe	Data Setup Time for WE	60		50		40		ns
23	ThD	Data Hold Time	30		20		15		ns
24	TrecWE	Write Recover Time	30		20		15		ns
25	TdisOwe	Output Disable Time from WE		90		75		50	ns
26	TdisOE	Output Disable Time from OE		90		75		50	ns
27	TenWE	Output Enable Time from WE	5		5		5		ns
28	TsuCwe	Output Enable Setup from WE	10		10		10		ns
29	ThCwe	Card Enable Hold from WE	10		10		10		ns
30	TsuCE	Card Enable Setup Time	0		0		0		ns
31	ThCE	Card Enable Hold Time	20		20		15		ns
32	TvWTwe	Wait Valid from WE		35		35		35	ns
33	TwWT	Wait Pulse Width		12		12		12	µs
34	TvWT	WE High from Wait Released	0		0		0		ns



Note: PC_REG is active Low for Attribute Memory reads only.

PCMCIA Write Memory Timing,
No Wait States

PCMCIA MEMORY WRITE TIMING (Continued)



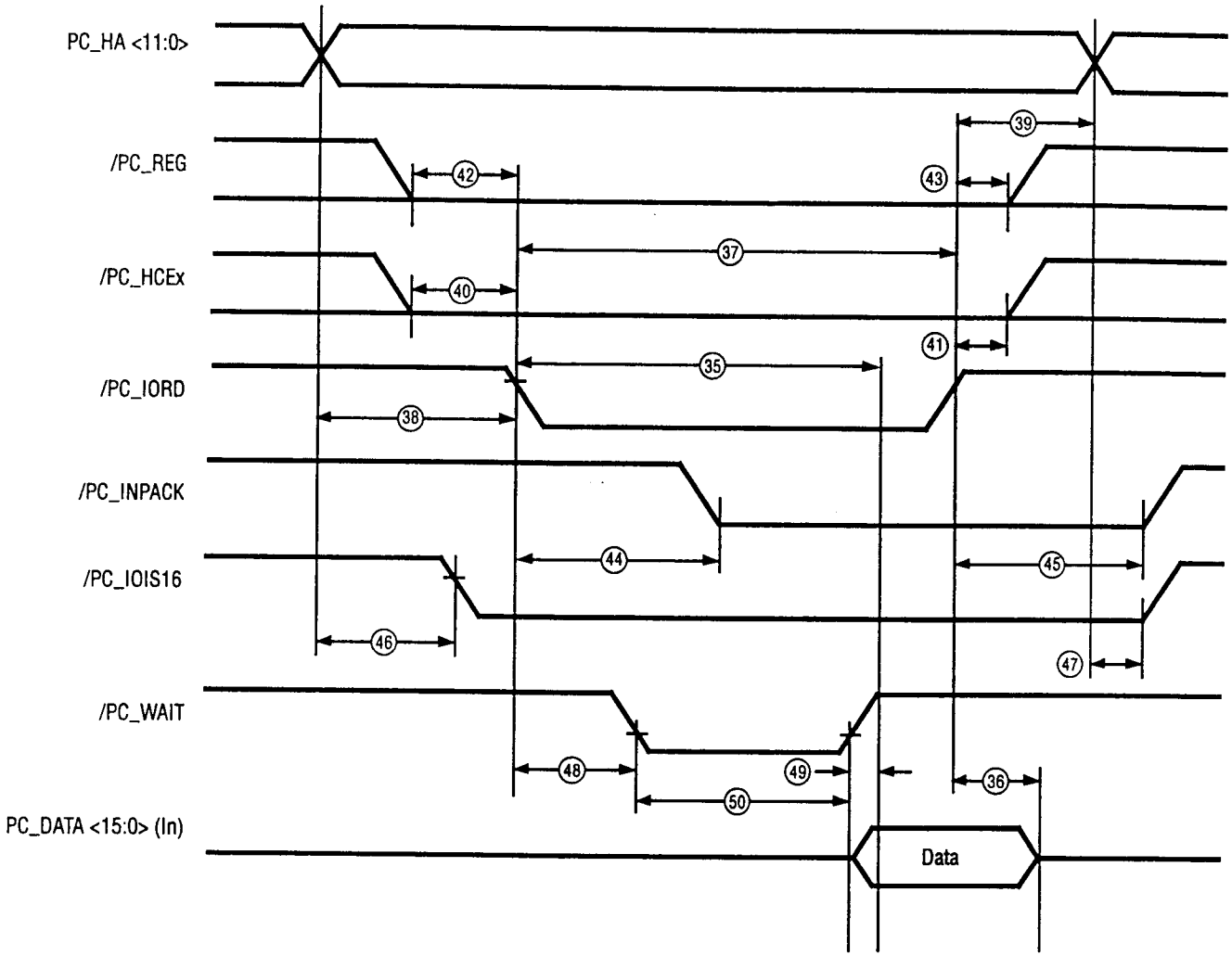
Note: /PC_REG is active Low for Attribute Memory reads only.

PCMCIA Write Memory Timing,
Wait State Enabled

I/O READ TIMING SPECIFICATION

No	Symbol	Parameter	Min	Max	Units
35	TdIORD	Data Delay After IORD	100		ns
36	ThIORD	Data Hold Following IORD	0		ns
37	twIORD	IORD Width Time	165		ns
38	TsuAiord	Address Setup Before IORD	70		ns
39	ThAiord	Address Hold Following IORD	20		ns
40	TsuCEiord	CE Setup Before IORD	5		ns
41	ThCEiord	CE Hold Following IORD	20		ns
42	TsuRGiord	REG Setup before IORD	5		ns
43	ThRGiord	REG Hold Following IORD	0		ns
44	TdIPKiord	INPACK Delay to IORD	0	45	ns
45	TdIPKiord	INPACK Delay from IORD		45	ns
46	TdIOISad	IOIS16 Delay from Address		35	ns
47	TdIOISadr	IOIS16 Delay Rise from Address		35	ns
48	TdWiord	Wait Delay from IORD		35	ns
49	TdWTr	Data Delay from Wait Rising		35	ns
50	TwWT	Wait Width Time		12	µs

PCMCIA MEMORY WRITE TIMING (Continued)

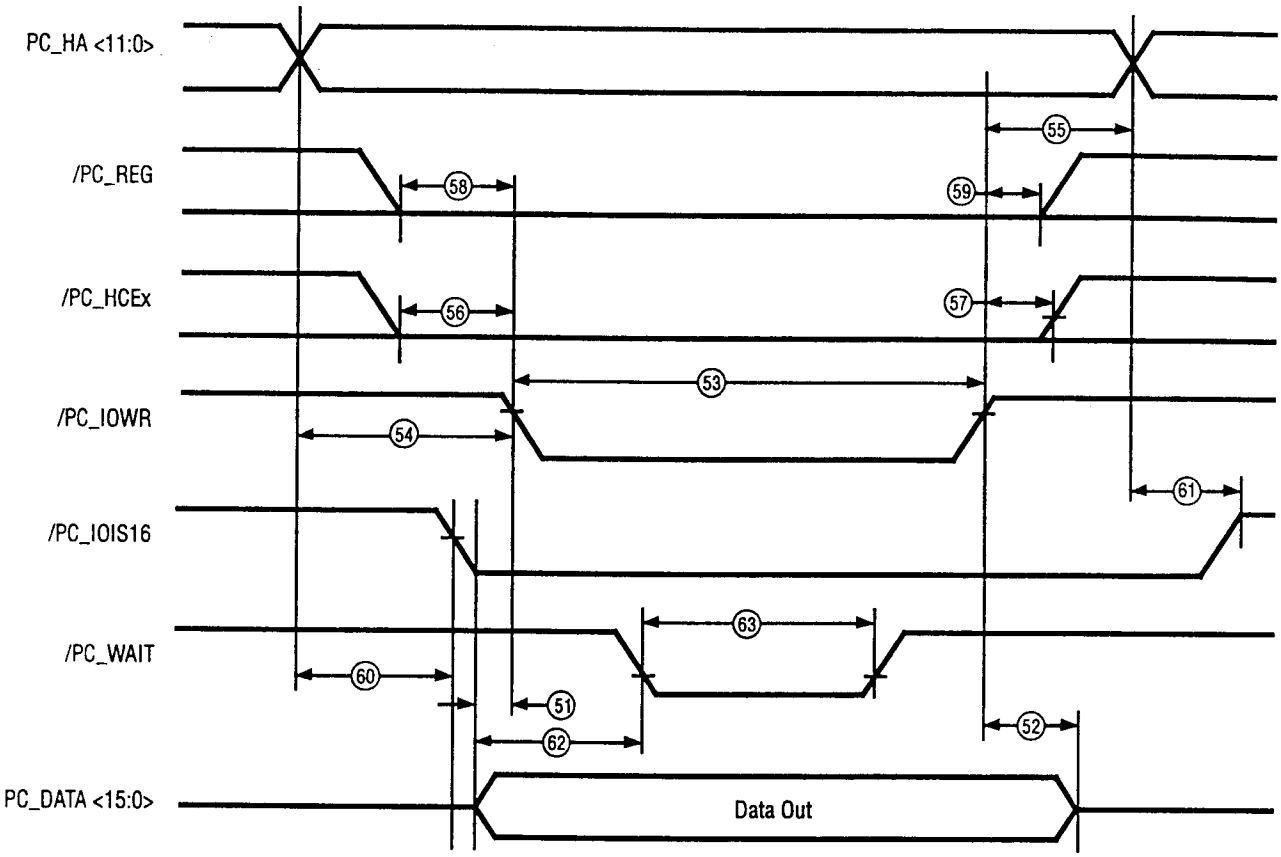


I/O Read Timing

I/O WRITE TIMING SPECIFICATION

No	Symbol	Parameter	Min	Max	Units
51	TsuIOWR	Data Setup before IOWR	60		ns
52	ThIOWR	Data Hold after IOWR	30		ns
53	TwIOWR	IOWR Width Time	165		ns
54	TsuAiowr	Address Setup to IOWR	70		ns
55	ThAiowr	Address Hold after IOWR	20		ns
56	TsuCEiowr	CE Setup before IOWR	5		ns
57	ThCEiowr	CE Hold after IOWR	20		ns
58	TsuRGiowr	REG Setup before IOWR	5		ns
59	ThRGiowr	REG Hold after IOWR	0		ns
60	TdIOISadr	IOIS16 Delay Falling from Address		35	ns
61	TIdIOISadr	IOIS16 delay Rising from Address		35	ns
62	TdWTiowr	Wait Delay Falling from IOWR		35	ns
63	TwWT	Wait Width Timing		12	µs

I/O WRITE TIMING SPECIFICATION (Continued)



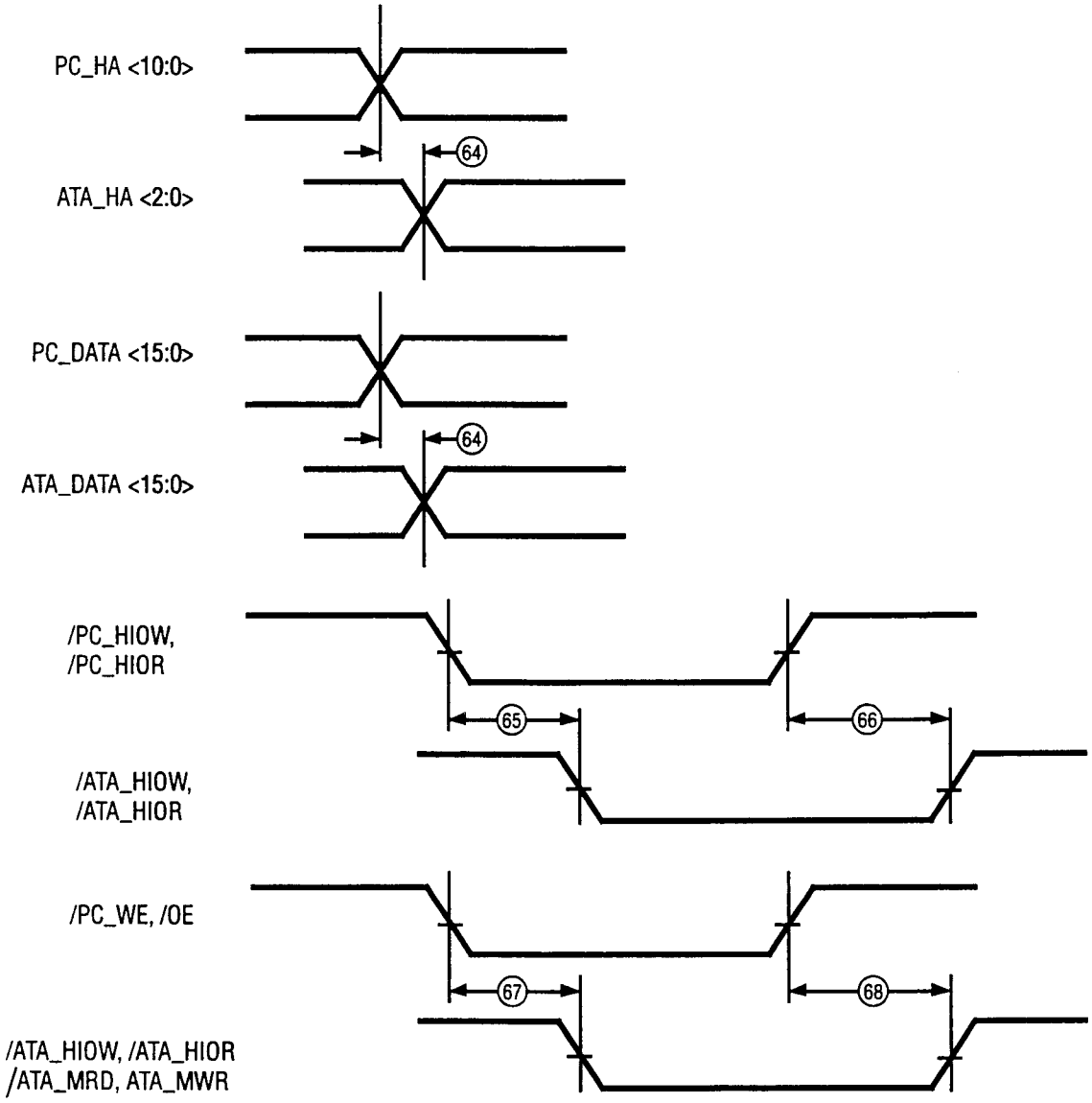
I/O Write Timing

Z86017BA DEVICE

SKEW Timing Between PCMCIA and ATA/IDE Or Peripheral Bus

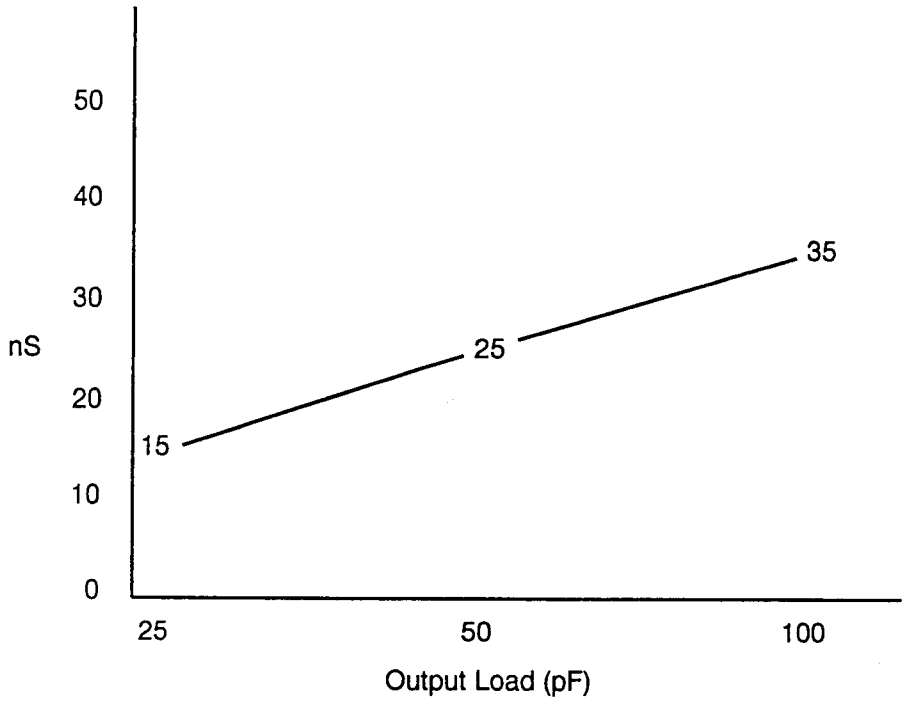
No	Symbol	Parameter	Min	Max	Units
64	TskADR	Address Skew		25	ns
65	TskI/Of	I/O Fall Skew		25	ns
66	TskI/Or	I/O Rise Skew		25	ns
67	TskMEMf	Mem Fall Skew		25	ns
68	TskMEMr	Mem Rise Skew		25	ns

50 pF Load



SKEW Timing Between PCMCIA and ATA/IDE or Peripheral Bus

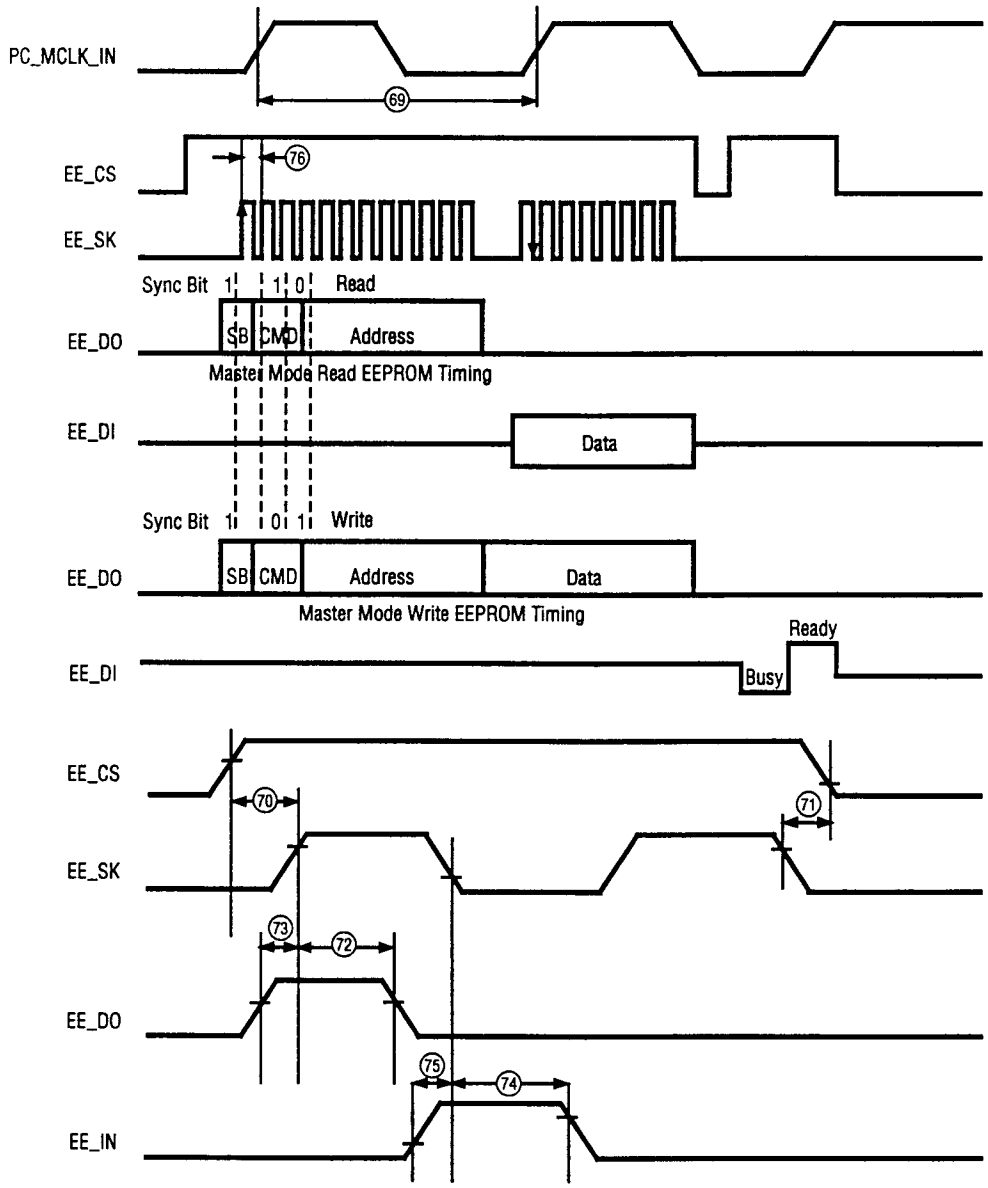
Z86017BA DEVICE (Continued)



Z86017BA Slew Delay Derating Curve (Typical)

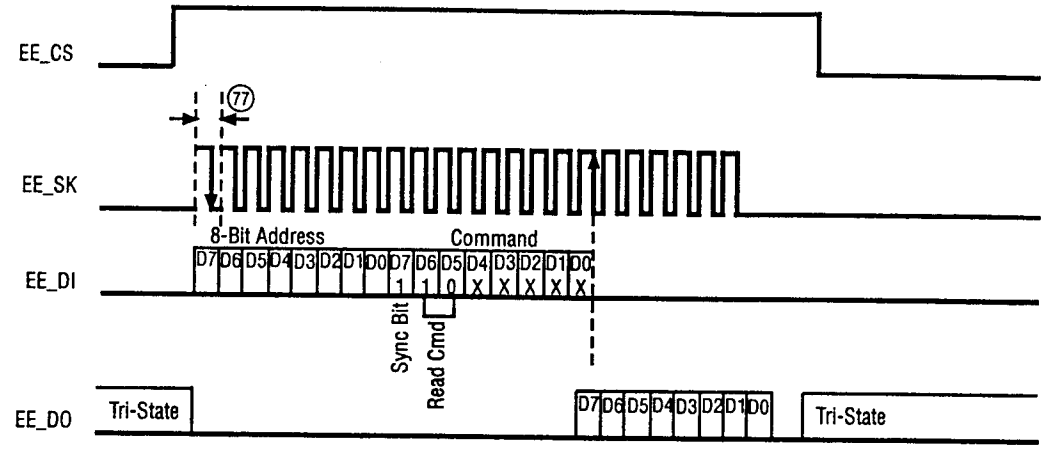
SERIAL INTERFACE TIMING

No	Symbol	Parameter	Min	Max	Units
69	TpMCKin	Master Clock In Period	50		ns
70	TsuCS	CS Setup to CLK time	25		ns
71	ThCS	CS Hold after CLK	0		ns
72	ThDout	Data Hold Time	10		ns
73	TsuDout	Data Setup Time	25		ns
74	ThDin	Data Hold Time	0		ns
75	TsuDin	Data Setup Time	25		ns
76	TpCKw	Clock Period, Master	200		ns
77	TpCKs	Clock Period, Slave	200		ns

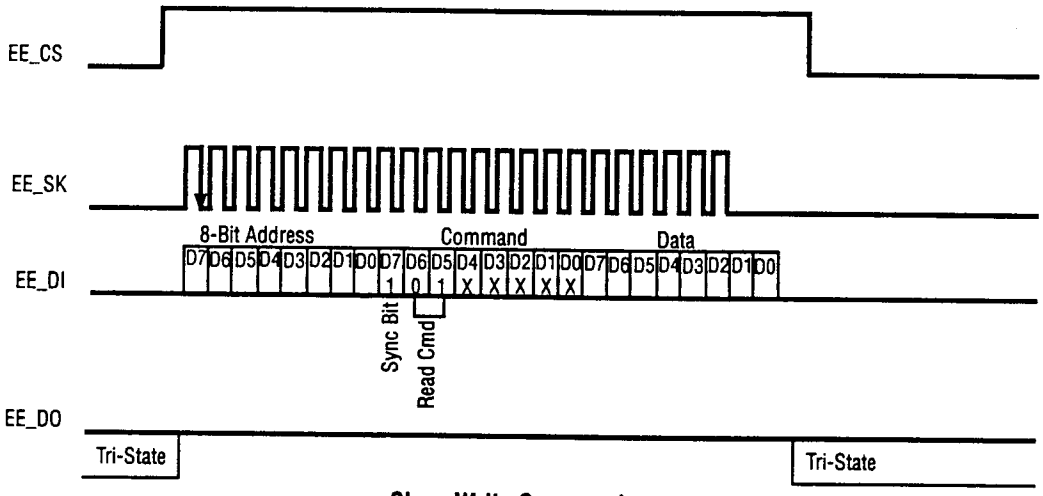


Master Mode Read EEPROM Timing

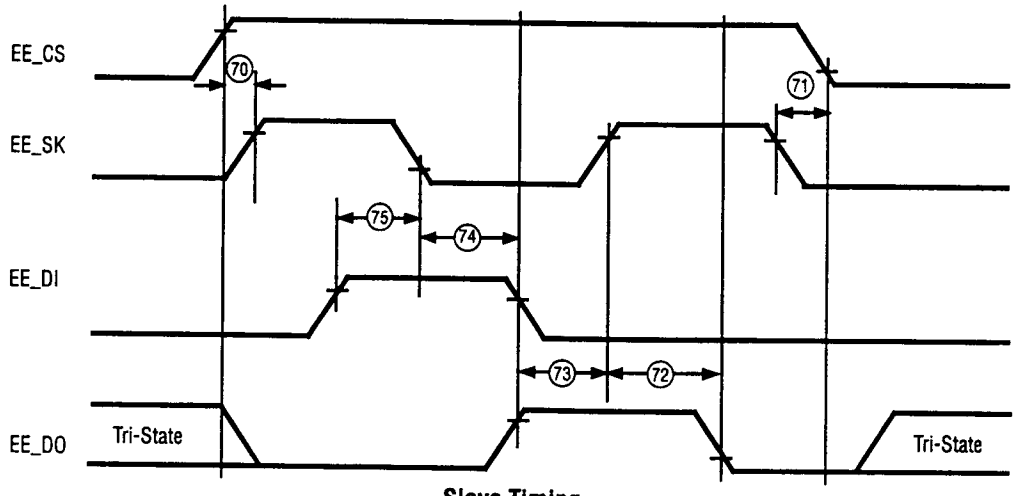
SERIAL INTERFACE TIMING (Continued)



Slave Read Command



Slave Write Command



Slave Timing

Slave Interface Timing (Read)

Z86017/Z86M17 OPERATING ERRATA

1) When the "EN_PADs" bit is set in register 2BH access to the CCR registers are disabled. Access to common memory and I/O space is still functional.

2) Setting the soft reset bit in the configuration option register will not be cleared out by a hardware host reset (PC_HRESET).

Standard Product:
Product acknowledged by Zilog to ship within thirty (30) days cannot be cancelled or rescheduled. This order will be invoiced for the full amount for all product cancelled or rescheduled within the thirty (30) days of the scheduled ship date.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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